IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION
Beacken-Pidwerbetski-Romain-Shively
CASE 5-4-2-17
TITLE Reducing Scintillation Effects for Optical Free-Space Transmission
APPLICATION NUMBER 09/839,486

THE COMMISSIONER FOR PATENTS
P. O. BOX 1450
ALEXANDRIA VA. 22313-1450

SIR:

AFFIDAVIT UNDER 37 CFR 1.131 by Dr. Richard R. Shively, co-inventor

In the United States of America
State of New Jersey
County of Morris

I, Richard R. Shively living at 5 Old Glen Road in the city of Morristown, county of Morris and state of New Jersey, being duly sworn, depose and say:

1. I have been employed by Lucent Technologies, Inc. or its predecessor companies since 1963. I graduated from the University of Illinois in the year 1963 with the degree of PhD in Electrical Engineering. I was designated a Bell Laboratories Fellow in 1982. My area of expertise is in communications signal processing and advanced communications and network design. My current assignment is in designing signal processing systems for U. S. government applications.

2. I am a named inventor or co-inventor on at least twenty issued U. S. patents.

3. I am a co-inventor of the subject matter claimed in the patent application captioned above with filing date of April 23, 2001.

4. I am personally familiar with the conception and development of the technology on which the subject patent application is based.

5. I have read the Amendment to this patent application to which my Affidavit is an attachment.

6. I submit this Affidavit for the purpose of establishing that the conception of the invention as claimed in claims 20 – 32, began in mid- 1999; and work in furtherance of the conception continued from mid 1999 through to the filing of the captioned patent application on April 23, 2001. To this purpose I offer the following evidence and testimony.

7. Some time in mid-1999 I conceived the idea of an improvement on interleaving an optical frequency data-bit stream for free space transmission, wherein the data stream is encoded with Reed-Solomon coding, the resulting codewords are segmented, and the segments are interleaved and read into a buffer store consisting of SDRAM devices

8. On or about July 14, 1999 my co-inventors Romain and Pidwerbetski participated in an in-house discussion sponsored by Lucent Technologies, Inc., at which various ideas for reducing scintillation effects accompanying optical frequency free-space transmission were advanced. A copy of a Summary of the July 14 1999 meeting made by Pidwerbetski is found on the last page of attached Exhibit "A".

9. Thereafter in August 1999 I and my co-inventors began working on the problem using such an SDRAM arrangement, of how to overcome the fact that the codewords are being generated in the typical case at a rate that with straightforward addressing for the interleaving will far exceed the maximum clock rate of state-of-the-art SDRAMS.

10. As this investigation proceeded my co-inventors and I came to realize that one can take advantage of the fact that SDRAM devices of high clock rate can READ and WRITE at the device cycle rate.

2.8 RRS

11. Thus, we realized, a remapping of codeword segment addresses such as by using consecutively addressed READ operands can be used to equalize the READ vs. WRITE rates, which means that even at a codeword generation rate of ~~20.8~~ gigabits/sec, a buffer store with a minimum number of SDRAMS will enable the interleaving to operate in real time.

12. As work on the project progressed, I recorded results in expectation of drafting a Memorandum to my management. By early in the year 2000 I commenced drafting the Memorandum under the title "MEANS FOR REDUCING SCINTILLATION EFFECTS FOR OPTICAL FREE-SPACE TRANSMISSION". The completed memorandum is attached as Exhibit "B".

13. To illustrate points made in the Memorandum, I constructed five figures of pictorial and graphical representations. These figures are attached as Exhibit "C".

14. I forwarded Exhibit "B" and "C" to colleagues.

15. On March 22, 2000 I emailed to Mr. Martin Finston, my patent attorney in the Lucent Patent Department suggesting "a new patent application" and attaching Exhibit "B" and Exhibit "C". A copy of the email to Mr. Finston is attached as Exhibit " D".

16. I have been shown a Lucent Technologies Patent Department "Submission Information" sheet marked Exhibit "E" and affirm that it refers to the opening of a patent submission to consider filing a patent application on the ideas of Exhibit "B" and "C".

17. On June 27, 2000 I and my co-inventors received an email from patent attorney Charles E. Graves stating that he had been assigned to write a patent application and asking for any other disclosure material describing the invention.

18. On June 28, 2000 co-inventor Alex Pidwerbetsky responded to Mr. Graves in an email attached as Exhibit "F". This email came with an attachment called "ERRCODE", which is Exhibit "A" to this Affidavit. Exhibit "A" contains some excerpts from proposal abstracts by which my Department was seeking funding to pursue development of ideas including those in Exhibit "B" and "C".

19. A first draft of the patent application covering the invention was forwarded to me by Mr. Graves bearing a date of 10/23/00. A copy of this draft is attached as Exhibit "G". I reviewed this draft and supplied comments to Mr. Graves.

20. There ensued one or more iterations of the patent application draft, one of which is alluded to in an email from Mr. Graves to me dated 5 Feb. 2001 entitled "final patent draft". A copy of this email is attached as Exhibit "H". The last draft of the patent application that I reviewed was dated on or around March 21, 2001.

21. To demonstrate that relevant portions of the disclosure of, Exhibit "B" are contained in the specification of the patent being applied for, the following examples are submitted:

a. The text under "DETAILS" p. 1 and 2 of Exhibit "B" is the same in substance as the text of the specification, p. 5 to 7.

b. Equations 1, 2 and 3 of the specification are those in the cited pages of Exhibit " B ".

c. P. 3 of Exhibit "B" includes the words: "While isolated references are made inefficient by the overhead described above, state-of-the-art SDRAMS devices can read or write at the device cycle rate within a page (i. e., row)". At p. 14 of the specification, these words are reiterated: "...the invention takes unique advantage of a characteristic of state-of-the-art SDRAM devices, which is that one can READ or WRITE to the devices at the device cycle rate within a page (i. e., row).

22. To demonstrate that the disclosure of Exhibit "C" is contained in the specification, the following examples are submitted.

a. Fig. 1 of Exhibit "C" is substantially identical to Fig. 3 of the drawings.

b. Fig. 5 OF Exhibit "C" is identical to Fig. 6A of the drawings.

c. Fig.3 of Exhibit "C" is similar in all material respects to Fig. 2 of the drawings.

23. Independent Claim 20 contains the feature quoted above from Exhibit "B":

".....each said SDRAM device having a cycle rate including a READ rate and a WRITE rate, and each said SDRAM device being both readable and writable at said cycle rate.... ".

24. Independent claim 32 contains several limitations found in Exhibit "B" including the disclosure at top of P. 4: "There is an opportunity to equalize these read vs. write rates and thus make the concept work in real time...". The corresponding language of claim 32 is:

"...said WRITE and said READ operations into and out of each said repeating x-y submatrix of said memory cells being conducted to substantially redistribute page change overhead operations from said WRITE operation to said READ operation, thereby to equalize the rate of said WRITE and READ operations...".

25. This ends my testimony.

Sworn and Subscribed to this date of 6-28-2004

IN the township of Whippany, County of Morris, State of New Jersey

Richard R. Shively

Dr. Richard R. Shively

NOTARY SEAL

Margaret Cardoso 6/28/2004

MARGARET CARDOSO
NOTARY PUBLIC
STATE OF NEW JERSEY
MY COMMISSION EXPIRES DECEMBER 2, 2008

"A" ERRCODE.doc

B.2 Link Margin / Transmission Rate Trade-Offs

The concept of reserving a Scintillation Margin to ensure a 10^{-9} Bit Error Rate is consistent with operating the free space optics link in the same fashion as fiber, i.e., synchronously. However, unlike fiber, free space is not a reliable medium but is subject to impairments such as the fading due to scintillations. An alternative idea would be to operate the free space optics link itself asynchronously with frames, acknowledgments, and buffering at the transmitter to allow frame re-transmission. Thus, instead of reserving a large margin for scintillations (e.g., 24 – 28 dB as for the long links in the calculations above) to avoid bit errors, reserve less and allow for the need to re-transmit some of the frames. This would enable a reduction in Scintillation Margin and allow these dBs to be applied to:

increasing range or
higher availability under less good weather conditions

at the expense of:

overhead for re-transmission / acknowledgment / CRC words
transmitter buffer memory
high speed CRC processing requirements

The transmitter would transmit a large number of frames while simultaneously storing them in a large buffer memory until successful reception of each is acknowledged by a reply from the receive end of the link. Cyclic Redundancy Check words would be inserted into each frame to establish data validity. If a frame is not acknowledged, within a certain period, it would be re-transmitted. The receive end would also buffer in order to insert re-transmitted frames as necessary.

As data from current Bell labs experiments becomes available it will be possible to empirically determine BER as a function of

Scintillation Margin as well as the temporal statistics of the scintillation fades (e.g., fading time scales). . Such data will indicate the number of dB that could be saved by operating at a higher raw BER, e.g., 10^{-4} instead of 10^{-9}. It would also indicate the frequency of re-transmits needed to maintain a 10^{-9} BER, potential frame sizes, buffer memory requirements, and the reduction in link capacity due to overhead.

An additional option to trade some transmission rate for improved link range / availability would be the use of high data rate error correction coding to improve receiver sensitivity. A codec capable of supporting up to 2 Gbps of data throughput is reported in the literature ("High Data Rate Error Correction Coding," D. M. Castagnozzi, etal., SPIE Proceedings, Vol. 2123, pp. 424 –433, Jan. 1994)

C.1.3 Option 3- "Smart" Protocol Realization / Test: Deliverables
The Baseline Program includes a "Smart" Protocol Design Task which uses the data from the link transmission experiments to design protocols having the potential to provide low BER with less link margin. The goal is to extend link availability to a wider range of atmospheric conditions and/or increase link length via intelligent algorithms that could be installed at the laser communication terminal's opto-electrical interface. Option 3 would carry the most promising algorithms / protocol designs from the baseline program into practice by development of prototype high speed ICs. The Option 3 deliverable would be a system test of the prototype components.

D.1.2 Design of "Smart" Protocols
As the data from the link transmission experiments becomes available this sub task will use it to design protocols having the potential to provide low BER with less link margin and thus extend link availability to a wider range of atmospheric conditions and/or increase link length. Such protocols would operate the free space optics link asynchronously with frames, acknowledgments, and buffering to allow frame re-transmission. They could also adapt transmission rate to atmospheric conditions to provide graceful degradation instead of link failure. In this case the link would still appear to be operating synchronously at its external interfaces but at a lower rate. Activities associated with this sub-task are:
Extract 1550 nm scintillation statistics from received power data
Design alternative data link protocols
Transmitter / receiver buffering
Framing / CRC
Acknowledge – re-transmit waiting times
Rate adaptation strategy
Potential Error Correction for Coding Gain

Do simulation analyses to quantify performance gains vs. protocol complexity
Size computing speed and memory requirements for implementation with evolving state of the art ICs
In coordination with DARPA ETO embedded signal processing initiatives

Task 1.3. Design of "Smart" Protocols for 1.550μm Optical Wireless

This task will use the link transmission experimental data to design protocols having the potential to provide low BER, with less link margin and thereby extend link availability to a wider range of atmospheric conditions and/or increase link length. Such protocols would operate the free space optics link asynchronously with frames, acknowledgments, and buffering to allow frame re-transmission. They could also adapt transmission rate to atmospheric conditions to provide graceful degradation instead of complete link failure. In this case, the link would still appear to be operating synchronously at its external interfaces, but at a lower rate.

Task 2.2 Design of Smart Protocols

The Baseline Program includes a "Smart" Protocol Design Task which uses the data from the link transmission experiments to design protocols having the potential to provide low BER with less link margin. The goal is to extend link availability to a wider range of atmospheric conditions and/or increase link length via intelligent algorithms that could be installed at the laser communication terminal's opto-electrical interface. This task would carry the most promising algorithms / protocol designs from the baseline program into practice by (1) development of prototype designs for high speed ICs and (2) system test of the prototype circuits or components via the OWTB links.

Constructive Plan

Design of "Smart" Protocols for 1.550μm Optical Freespace Systems

Lucent Technologies shall perform level of effort system engineering support to design protocols to provide low BER with less link margin and extended link availability, for a wider range of atmospheric conditions and/or distance. These protocols will operate the free space optics link asynchronously with frames, acknowledgments, and buffering to allow frame re-transmission. Lucent shall assess transmission rate dependence on atmospheric conditions to provide graceful degradation instead of link failure. Considerations associated with this task are:

1.550μm scintillation statistics from received power data
Design of alternative data link protocols
Transmitter / receiver buffering
Framing / Cyclic Redundancy Check (CRC)
Acknowledge – re-transmit waiting times
Rate adaptation strategy
Potential Error Correction for Coding Gain
Simulation analyses to quantify performance gains vs. protocol complexity
Computing speed and memory requirements for implementation with state of the art IC.

Development of Smart Protocols and Networking Test

Lucent Technologies shall perform level of effort engineering system support for development of smart protocols and networking tests. The Baseline Program includes a "Smart" Protocol Design Task which uses the data from the link transmission experiments to design protocols having the potential to provide low BER with less link margin. The goal will be to extend link availability to a wider range of atmospheric conditions and/or increase link length via intelligent algorithms that could be installed at the laser communication terminal's opto-electrical interface. Results from option task 2.2 will be utilized for integrating algorithms / protocol designs from the baseline program and will be used to system test

the prototype components. This task would develop the board level components needed to realize the Smart Protocol sub-system.

Performance tests will be conducted to measure the reduction in Scintillation Margin that could be achieved and associated performance enhancements. Results will be integrated into the OWTB.

Summary from July 14, 1999 OpticsAir brainstorming session:

The intent of the OpticAir brainstorming session was to surface ideas to increase availability and decrease cost. Having done this, it was suggested that each identified area of improvement be assigned to a subteam comprised of attendees, and others, who would meet as a group in the next month, and more formerly defined the scope of work and funding support required to pursue these avenues of interest.

Transmission protocols and error correction may be capable of improving performance when atmospheric conditions are marginal.

Suggested team for leading this effort:
Alex Pidwerbetsky
Dennis Romain

"B"

MEANS FOR REDUCING SCINTILLATION EFFECTS FOR OPTICAL FREE-SPACE TRANSMISSION

INTRODUCTION: The notion of interleaving (shuffling) data streams to achieve greater robustness in communication applications is well known. Succinctly stated, "a *t*-error-correcting code interleaved to degree *i* is capable of correcting all single bursts of length *it* or less." * The advantage stems from the fact that many communication errors occur in bursts, and the result from a burst error can be made to have the effect of many isolated errors if the data is interleaved over a span large compared to the burst duration.

The purpose of this note is a description of an implementation that could extend the error correction capabilities of Optic Air to bursts of ***20 million* consecutive bits**, and thereby mask most bursts in some applications, at the cost a) a few hundred dollars in parts, b) 200 milliseconds of added latency which would have negligible effects in data and broadcast video applications, and c) a 14 % overhead in terms of check symbols.

A novel structure is selected as a demonstration to leverage the inexpensive cost of dynamic-random-access-memory (DRAM) technology. Specifically addressed is the very large overhead associated with changing pages (i.e. DRAM row address) each memory reference when address strides in row-column matrix addressing are large compared to the page size. A distributed remapping of addresses mitigates the effect and enables real-time operation that would otherwise not be possible in the example application.

DETAILS: Specifically the process is as follows:

a) encode the data stream in codewords (i.e. blocks) of **n** bits (comprising **k** payload bits and **(n-k)** error-correcting-code bits) ; define the maximum number of errors that can be corrected within a codeword as **b**; {the maximum number of bits that can be corrected by *any* linear code is: **b = .5 *(n-k),** and that is the property of the Reed-Solomon code being proposed (see Theorem 4:15, Peterson and Weldon)}

b) define the maximum error burst to be masked as **E** bits in duration;

c) then the burst error can be masked if **M** codewords are interleaved, where

$$\mathbf{M = E / b}$$

d) the span of the interleaving (the dimension of the permutation matrix, i.e. size **S** of the buffer required and hence the duration of the latency added by this process) is therefore:

$$\mathbf{S = M * n.}$$

* W. W. Peterson, E. J. Weldon. *Error Correcting Codes,* MIT Press, p. 371,

The process is illustrated in Fig. 1. After the payload is encoded into codewords, the codewords are fragmented and distributed over the buffer, interleaved with other codewords, over a span sufficiently large that a burst error E bits in duration will affect at most b bits in any given codeword. (It is assumed that the scintillation fades are sufficiently infrequent such that two or more do not occur within one interval of S bits. Isolated random errors that might also occur in the vicinity of the maximum sized burst are also ignored, although this issue could be addressed by concatenating an inner code if needed. Also ignored in this exposition is the negligible effect, in terms of sizing, of the error burst starting or ending in the middle of a codeword fragment.)

Assume the code in question is Reed-Solomon using a Galois Field of 8-bit symbols and that the (255,223) code is used; this means a codeword is 255 octets (bytes) in length, of which 223 are payload, with the remaining 32 as check symbols. The code has the capability of correcting 32/2 or 16 bytes of error. This means that as few as 16 isolated errors (i.e. if each error were in a different octet) could be corrected, but that as many as 16 x 8 or 128 bit errors would be corrected in any block if the errors all occurred within 16 bytes.

In a field measurement of free-space optical transmission over a 10 km range by AstroTerra, they showed a histogram that appeared to indicate roughly 90% of the fades were of duration less than 8 ms. (Unfortunately, they did not show a cumulative distribution. The actual results would of course be dependent on weather and other effects.)

A bit rate of 2.5×10^9 /sec. would yield a value of $E = 20 \times 10^6$ bits lost during an 8 ms. fade.

Since at most 128 bits of any codeword can be lost due to the burst error and still mask the burst, the number of codewords that must be interleaved is

$$E / b = 2 \times 10^7 / 128 = 156250.$$

Since the codeword is 255 x 8 = 2040 bits long, this implies an interleaving buffer size of:

$$(E / b) * n = 156250 * 2040 = 318,750,000 \text{ bits.}$$

This may sound large until one realizes that commodity DRAMs of 128 megabits in size are under $20, and 256 megabit DRAM devices are available.

An implementation of the interleaving process is illustrated in Fig. 3. Sixty-bit sections of the codeword were chosen because 60 is an integer factor of 2040, and 60 bits x 156250 x 2 is close to the 20 megabit burst (18.75 megabits). (The shift register need not actually operate at 2.4 GHz. since a parallel-serial structure could be realized.) A burst error of that duration would destroy two 60-bit sections (<128) of each of 156250 interleaved codewords, and therefore all of the data would be recovered.

ADDRESSING DETAILS: The interleaving process is equivalent to a matrix transpose; specifically consider (for the set of numbers used in this instance) a matrix of 156,250 rows x 34 columns, with each matrix entry a 60-bit section.

Implementing the interleaving with static RAM devices would be conceptually trivial, but *practically* the largest SRAM available in the speed range required is 18 megabits (requiring roughly 40 such devices to realize a 320 megabit double buffer) and the device cost is quite high (order of $100). Address-signal loading, power, and system reliability simply because of the large device count would be further complicating issues.

Performing interleaving in a straightforward manner would suggest writing entries at address increments of 156250 (i.e. matrix column entries), then reading out consecutive addresses (rows) to transmit the interleaved codewords. Parameters peculiar to state-of-the-art SDRAM (Synchronous DRAM) make this difficult, because of latency effects vis-à-vis isolated read (or write) operations. Forming 60-bit words in Fig. 3 requires 20.8 ns (60 times the bit period of the 2.8 x 10^9 bit/sec. encoded data stream). With SDRAM devices with a CAS-latency of 2, the maximum rate of writing into distinct rows (pages) of DRAM is once every 7 cycles. (E.g. see data sheet for Micron technologies SDRAM, device no. MT48LC8M16A2,revision 11/99, p 50.) The 7 cycles involve:

a) issuing an ACTIVE command to activate the bank and row,

b) issuing the column selection, WRITE command and write data two clock cycles later,

c) then, after three more cycles, issuing a PRECHARGE command to de-activate the bank,row selection just made, and after two additional clock periods the cycle is repeated for the next ACTIVE command.

The fastest CL-2 SDRAM currently available has a maximum clock rate of 133 MHz., or 7.5 ns. cycle time. Clearly the seven cycle write epoch is not compatible with 20.8 ns. rate at which new 60-bit codeword sections are being generated. Commutating among multiple banks of memory devices would be one way to address this speed problem, but multiple devices are not required from a capacity point of view and therefore other approaches would be far preferable.

While isolated memory references are made inefficient by the overhead described above, state-of-the-art SDRAM devices can read or write *at the device cycle rate within a page (i.e. row).* For the Micron SDRAM device cited earlier (with 16 bits x 2M x 4 banks) the page size is 512 sixteen-bit words, and the clock rate is 133 MHz. (7.5 ns).

Therefore, addressed in a straightforward way, these devices would require 7 x 7.5 = 52.5 ns. per write (because the write address increment far exceeds the page size) while consecutively-addressed read operands could asymptotically be performed at a 7.5 ns. rate, well under the 20.8 ns. rate required.

There is an opportunity to equalize these read vs. write rates and therefore make the concept workable in real time with a minimum number of SDRAM memory devices by remapping memory addresses. The strategy described in what follows is to a) regard each page in SDRAM memory as multiple "virtual" pages, and b) exploit the fast WRITE rate on the same (physical) page in exchange for requiring a more frequent page change during READ in the permutation operation.. The general approach is to write K consecutive entries *into one physical page*, with the result that the "read" process must then change pages [P/K] times as often (where P is the page size) compared with simply reading each P-entry page of SDRAM as a single sequence of consecutive addresses.

For the numbers involved in the example define each physical 512-word SDRAM page as consisting of 34 pages of 15 words each (two words are wasted). Recall that the permutation matrix is 34 x 156250 in size, and therefore 34 is selected to make indexing systematic. (In this particular combination of numbers, the "write" process in the interleaving operation does not have to change pages at all before a physical page is full,)

The remapping of addresses is indicated in Fig. 5. During the WRITE operation, entries 1,1 1,2 .... 1,34 are stored in physical addresses 0,15,....,495 of the first SDRAM page, but these are to treated during "read" as addresses 0, 156250,.....,33x156250 respectively. Because the factorization of addresses maps has the row length as one factor, exactly 15 rows of 34 entries fit in one first physical page. The "virtual" addresses referred to in Fig. 5 refer to the sequence in which the read-out is performed to complete the permutation.

Because of the 7-cycle overhead when a page change does occur (@7.5 ns/cycle) versus the 20.8 ns. system cycle rate, a first-in-first-out elastic memory of 4 entries provides a means to bridge the page change. The 52.5 ns. interruption incurred by the page change is effectively masked with a backlog of 3 entries in the elastic memory.

"C"

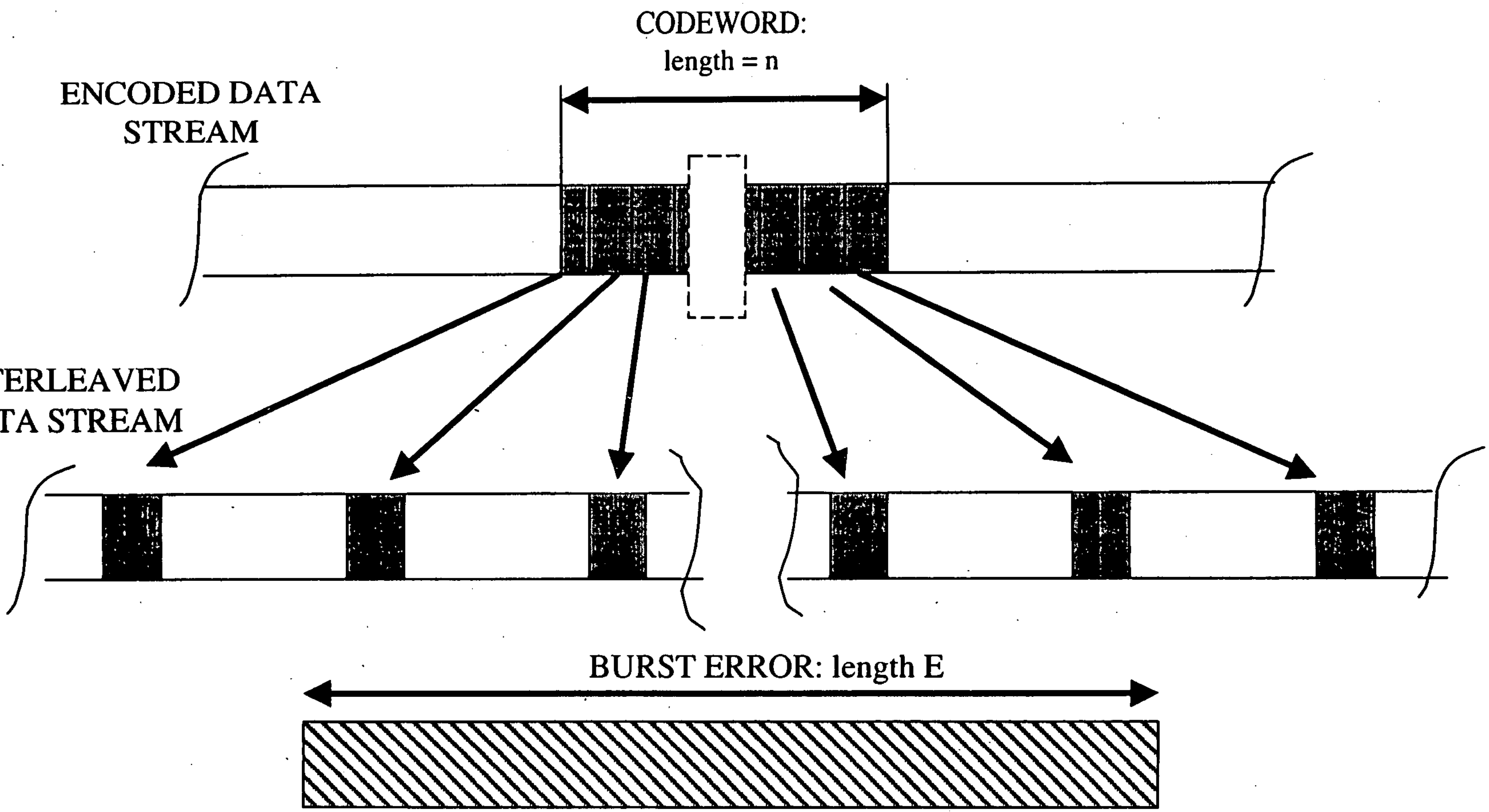


FIG. 1: Interleaving the Encoded Payload

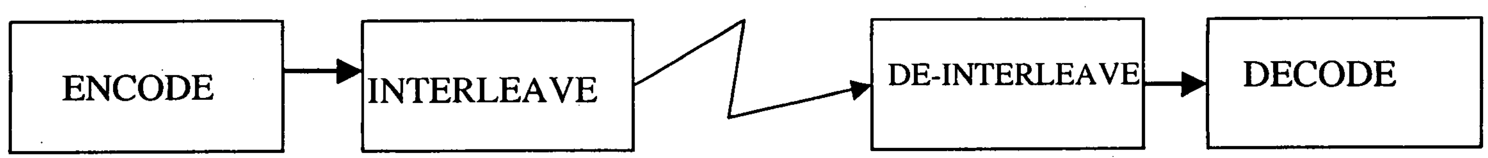


Fig. 2: Processes Involved

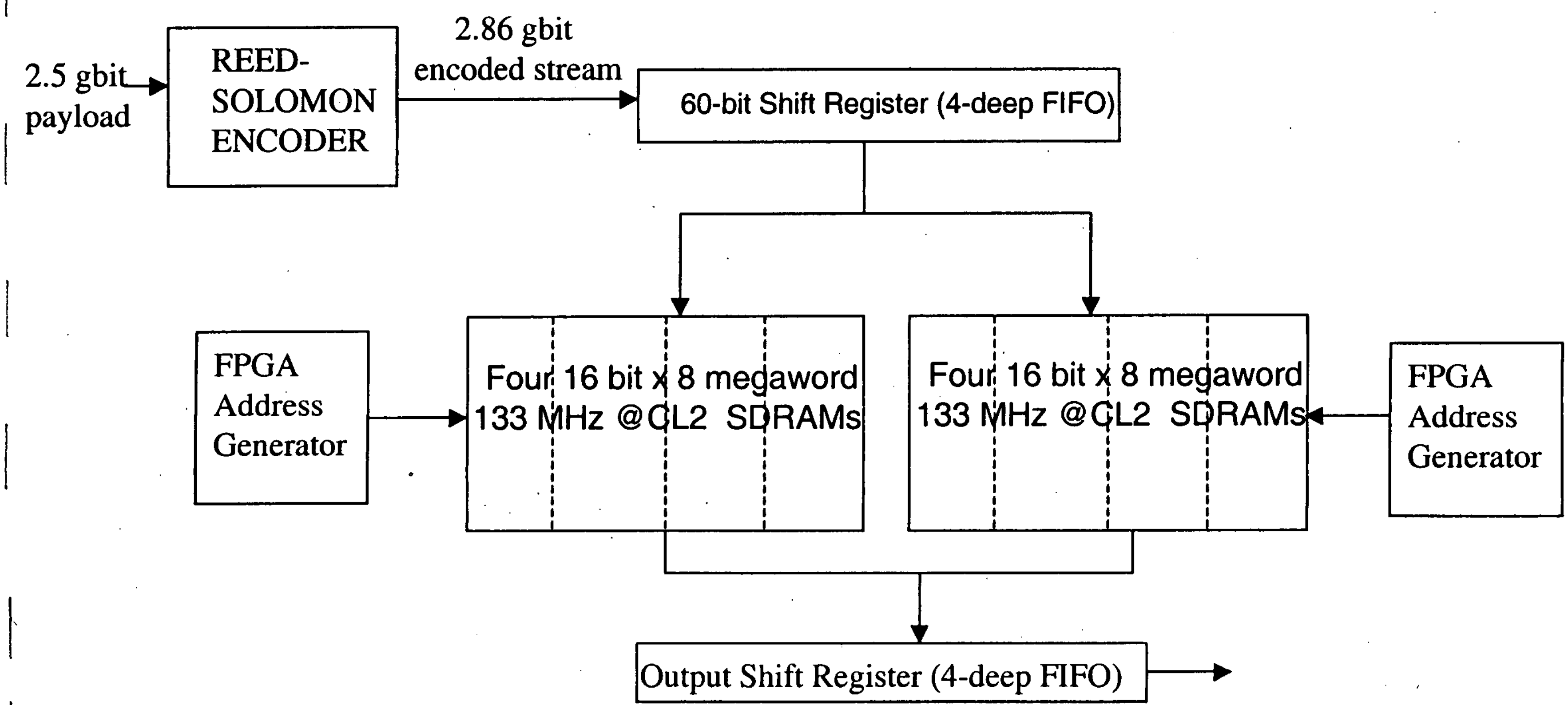


Fig. 3 Example Realization of Transmit Circuitry to Mask Scintillation Fades

Denote the 60 bit segments of the codewords by a 2-tuple:

(n,m): n = codeword number; m= 60-bit segment within the codeword indicated
n = 1,2,...,156250
m = 1,2,...,34 for 2040 codeword length

Then after interleaving the first block of 156,250 codewords the sequence is:

[1,1 2,1 3,1 ......156250,1] [1,2 2,2 ....156250,2] .... [1,34 2,34 ... 156250,34]

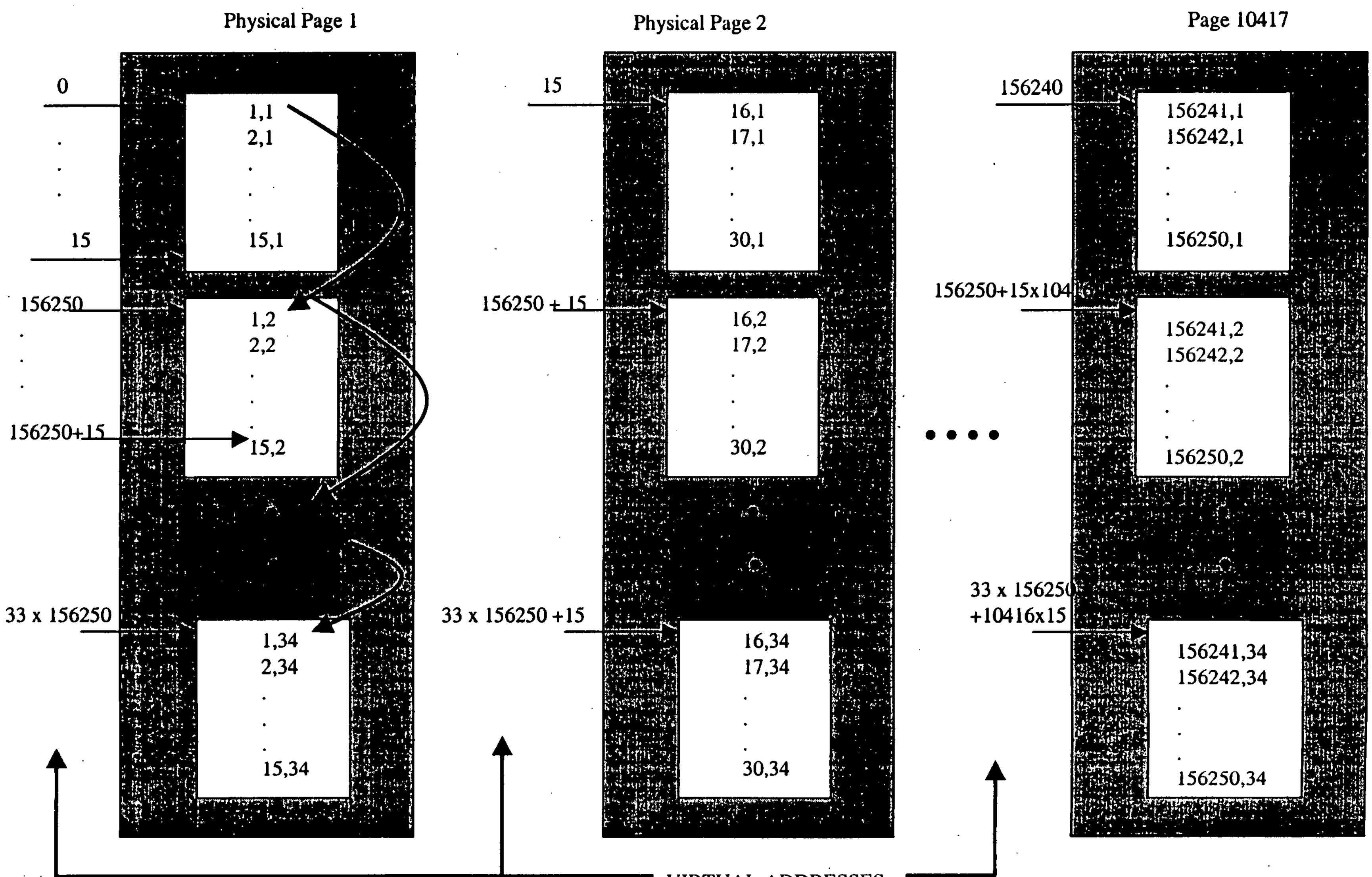
(brackets included only to clarify the writing of "column entries" for subsequent read-out as rows.)

Note that consecutive entries from the same codeword are separated by 60 x 156250 =9.375 megabits; An erasure of any two if the bracketed sequences (each 9.375Mbits) incurs no more than 120 bits of error in any codeword.

FIG. 4: Interleaving in the Example Used

Figure 5: Remapping Addresses to Balance "Read" vs. "Write" Overhead in Terms of SDRAM Page Changes

(Virtual pages are 15 words in length)



"D"

Finston, Martin (Martin)

From: Shively, Richard R (Richard)
Sent: Wednesday, March 22, 2000 4:03 PM
To: Finston, Martin (Martin)
Cc: Beacken, Marc J (Marc); Pidwerbetsky, Alex (Alex); Romain, Dennis M (Dennis); Auborn, James J (Jim)
Subject: A new patent application

Martin:

There is some interest in the use of free-space optics to provide high-capacity (2.5 gbit and higher) short-haul (~10 KM) links. In addition to Lucent's recent Optic Air product, Dan Hesse (formerly head of AT&T wireless) just left AT&T to head up a company in this area. Many vendor personnel, with significant knowledge of what Lucent is doing in this area, joined this company so some further patent protection would be worthwhile.

A critical problem, even on nice weather days, is turbulence as it effects light refraction and induces fades, typically quite short (order of a few milliseconds). At multiples of 2.5 gigabits/sec. this leads to the loss of lots of bits.

The proposed invention addresses this issue.

Viewed otherwise, the Optic Air system includes a very significant margin in its loss budget (20 dB) to limit but not eliminate this effect. Since lasers are roughly proportional to power level in cost, this adds significantly to that element of the system cost. Therefore a feature that could reduce the power capacity required to achieve a given performance would not only reduce overall cost but also mitigate safety issues that limit power levels allowed (and hence range achievable) because of human exposure hazards.

I would propose the following co-inventors: Marc Beacken, Alex Pidwerbetsky, and Dennis Romain.

The attached two files provide the initial text and diagrams to describe what is proposed.

Richard Shively

FEC for optic air3.doc

FEC for optic air.ppt

SUBMISSION INFORM..ION "E"

Attorney: Martin I. Finston

Submission Title: Method Of Optical Free-Space Communication Having Improved Resistance To Scintillation Effects

Filing Deadline:

CLASS II

Date Received From Inventor(s): 3/22/00

PLEASE SUPPLY WHATEVER INFORMATION IS <u>READILY AT HAND</u>:
(If additional space is needed, please use a second sheet)

INVENTOR: Beacken | M. | J.
Last | **First** | **Middle**

SSN (if known):
Organization No.: 630041000

INVENTOR: Pidwerbetsky | A. |
Last | **First** | **Middle**

SSN (if known):
Organization No.: 630041000

INVENTOR: Romain | D. | M.
Last | **First** | **Middle**

SSN (if known):
Organization No.: 630041000

INVENTOR: Shively | R. | R.
Last | **First** | **Middle**

SSN (if known):
Organization No.: 630041000

Please attach all paperwork desired to be bound into folder.

PT 360.subinfo (10/97)

NEW PATENT SUBMISSION

Inventors: Marc ~~Beaken~~ Beackon, Alex Pidwerbetsky, Dennis Romain, Richard Shively

Title: Method of Optical Free-Space Communication Having Improved Resistance to Scintillation Effects

Date disclosed to Patent Attorney: March 22, 2000

Government Contract? No

Statutory Bar? No

Subject Code: 5S

Brief Description:

Problem: Turbulence causes loss of message bits during free-space optical transmission. Solution: An adaptation of the known method of interleaving data streams to extend the error-correcting capabilities of Reed-Solomon coding.

Code II

X-Sender: alex@mail.gsrd.lucent.com
Date: Wed, 28 Jun 2000 11:28:09 -0400
To: Charles Graves <jgraves@austin.rr.com>, rshively@lucent.com,
dromain@lucent.com, pidwerbetsky@lucent.com, marc@lucent.com
From: Alex Pidwerbetsky <pidwerbetsky@bell-labs.com>
Subject: Re: patent application

Charles:

Here is some more supporting infomation on this patent application.
I am sending it to the other inventors so that they can comment, if need be, on my answers.

Q1: Attached is a file (Errcode.doc) with extracts from proposal abstracts, proposals and the July 14, 1999 OpticAir technology brainstorming sessions. The extracts cover proposed work on dealing with scintillations using coding and protocols, so that on the order of 20 dB of margin would not need to be reserved in the link budget for scintillations. Although the brainstorming session reached a consensus that coding and protocols needed to be pursued, it never got above the funding line. Same for the proposals. The writing was done between Dennis Romain and myself.

Also there is this email (from me to Dom Imbesi et al) extract on correlation time scales for scintillation fades which the coding would need to cover:
The analysis that Dennis Romain has done on the limited data set obtained so far indicates that the temporal correlation of scintillation is on the order of 15 millisecond. This is for a range of 4.4 km and a crosswind (that I reduced from the data) on the order of 10 mph. For a range of 1 km, that time scale should then scale to 7-8 milliseconds. Additionally, if the crosswind is 20 mph, it becomes 4 milliseconds.

I can go through the scaling, if you are interested.
If there is anything else I can do to help, please let me know.

Q2: Yes, we are all inventors on this patent.

Q3: We are looking for funding to push this work forward, however, there is no current work ongoing that is likely to produce new results on this topic in the next 2-3 months.

Q4: No current papers are being written by us on this topic, although we would like to do so in the future. This would be after the August 15, 2000 submittal date.

Q5: There is extensive prior art in the RF wireless domain (note that this is a different physical layer as well as different propagation), where because
the data rate is lower, the number of bits covered is much less. This raises an interesting question about extending the claims for this patent also into the RF wireless domain in anticipation of much higher RF wireless data rates which would lead to a large number of bits being dropped in a RF fade.
There is also current work (including a significant Lucent effort) on error coding
for fiber optic communications, but this is for individual bit errors, not the large
burst of errors described in this disclosure.

As to question 6: OpticAir is the free space optical communications product that Lucent was developing prior to the TeraBeam joint venture deal.
However,

the reference to Optic Air in Dick Shively's write-up is generic. This
invention
applies to free-space optical communications in general, not just the
OpticAir
product.

Hope all of this helps. If you need anything else, please contact us.

Alex

At 01:29 PM 06/27/2000 -0500, Charles Graves wrote:
>Dick, Dennis, Alex, Marc:
> You probably know that I have been assigned to write the patent on
>your invention disclosure "Means for Reducing Scintillation Effects for
>Optical Free-space Transmission". Here are a few initial questions, before
>I put pen to paper.
>1. The disclosure material I received is a 4-page memo of the same title
>authored by Dick, plus figs 1, 2, 3, 4, 5. Question is: Is there any
>further, reasonably coherent, material in any of your files that I ought to
>have in order to write the application? E.g., lab notebook entries, tests,
>etc.?
>2. Am I right to assume that if we based the application solely on Dick's
>memo material, all of you would be listed as inventors?
>3. Do you plan additional work, or writing, or research in the near f uture
>(2-3 months) on the subject of the invention? If so, do you expect any
>further material would arise from such work that we would want to include
>in the patent application?
>4. Do you plan to publish? If so, when do you need to submit the article
>and to whom? (My instructions are to have the application filed by Aug. 15,
>2000-which could be a publication date).
>5. I note that the invention extends the error correction capabilities of
>Optic Air to bursts of 20 million consecutive bits - at some cost of add'l
>parts, some added latency, and some more overhead. If you know of an
>issued patent or published article that would serve as an example of the
>prior art where the error correction capability is less, could you provide
>a copy? If you don't have a patent or article in hand, don't worry about it.
>6. Am I right that the term "Optic Air" just refers to the general
>atmospheric optical transmission medium, or is it a more precise term of
>art?
> Good to be working with you again.
>ceg
>
>
>
Attachment converted: Rich:Errcode.doc (WDBN/MSWD) (00090334)

" G "

Submitted to K.S. 10/23/00

TITLE OF THE INVENTION

REDUCING SCINTILLATION EFFECTS FOR OPTICAL FREE-SPACE TRANSMISSION

BACKGROUND OF THE INVENTION

Optical free-space transmission is subject to degradation arising from the effects of scintillation in the transmission medium. Free-space optical signal experiences fades from scintillation over times on the order of several milliseconds. During these times, a multi-gigabit/second signal may loose tens of millions of bits. For example, an 8 millisecond fade in a 2.5 gigabit/sec. data stream equates to the loss of 20 million bits.

When a data stream is transmitted over optical fibers, block-oriented forward error correction (FEC) is widely used. However, the degradation arising from scintillation effects in free-space optical transmission can last for millions of bits compared to the typically far shorter duration of error bursts in optical fiber media. The single-block FEC error correction process is extremely impractical in correcting errors of the lengths that may occur in free-space optical transmission.

Addressing the problem resulting from scintillation effects by selective re-transmission of affected blocks is also not practical for such large error

bursts, due to the real-time nature of communication processes such as video. Cost, size, and power consumed by the correction process must also be constrained in realizing a commercially practical communication terminal.

The practice of interleaving, or shuffling, data streams is used to achieve greater robustness and noise reduction in many communications applications. The general principle, as stated in the publication "Error Correcting Codes", W. Peterson and E. J. Weldon, MIT Press (1972), p. 371, is that a ***t***-error-correcting code interleaved to degree ***i*** is capable of correcting all single bursts of length $i*t$ or less. Through interleaving, the burst error can be made to have the effect of many isolated errors, provided that the data is interleaved over a span large compared to the burst duration.

Accordingly, there is a need in current optical free-space transmission for error-correction processes which can correct for error bursts that last for tens of millions of consecutive bits. However, in correcting tens of millions of bits in a burst error within a single code block, the communication terminal cannot practically use the extraordinarily large encoder/decoder that would be required under current terminal design concepts.

Synchronous-dynamic-random-access-memory (SDRAM) devices are available that can provide a practical means of implementing the large permutation matrix capacity required. However, SDRAM devices incur multiple cycles of delay whenever it is necessary to change the "row" address in the row-column addressing that is intrinsic to SDRAM

implementation. The SDRAM rows, hereinafter termed "pages", typically incur a significant, multi-cycle overhead cost whenever it is necessary to change the row address, i.e. change "pages". The column address field typically equates to the low order digits in the physical address of the SDRAM, such that when addressing consecutive or grouped sets of data, a minimum of page changes is incurred. If the SDRAM devices were addressed in a straightforward way, namely storing segments of the block FEC codeword in successive addresses, then read-out of this codeword sequence in permuted order to effect the interleaving would require changing page addresses every memory reference due to the large address increments required. An analogous process is that of storing a matrix with row elements in successive addresses, then reading the matrix by column. Address increments equal to the row length would be required in reading the transposed matrix. In a typical SDRAM device where seven cycles are required to change page addresses, the permutation would result in a seven-fold reduction of the effective memory speed. Because the high bit rates involved in optical communications already mandate using the fastest SDRAM devices available to perform this interleaving process, such a slowdown would impair the practicality of implementing the process

SUMMARY OF THE INVENTION

This invention is a novel structure and process for encoding an optical data stream subject to transmission degradation from scintillation effects. Using, as one sample, Reed-Solomon coding, a payload bit stream is encoded and the resulting codewords are fragmented over a relatively large span for interleaving. The invention uses existing SDRAM components for permutation buffers. However, the invention overcomes the limitations of

SDRAM devices with respect to supporting large array permutations by means of a mapping of virtual addresses of the permutation buffers onto the physical addresses of SDRAM. The fragments are written into designated addresses in the SDRAMs. To equalize an inequality of the READ vs. WRITE rates, a distributed remapping of addresses is performed. (Many equivalent mappings exist; the example presented hereinafter is for purposes of illustration.) The intended result is that the overhead associated with row-address changes is roughly equal in both the WRITE (i.e. input to the permutation buffer) and READ (read-out of the permutation buffer). In this way the overhead cycles can be amortized over a large number of memory references for both the read and write process, such that the effective memory cycle rate asymptotically approaches the burst physical cycle rate.

The remapping involves treating each physical page (row) in SDRAM memory as multiple "virtual" pages, which establish the sequence for READOUT to complete the permutation. The typically very large overhead associated with changing pages with each memory reference when address strides in row-column matrix addressing are large compared to the page size, is substantially reduced.

The invention thus solves the problem of economically managing the very large interleaving or permutation span required to cover error bursts of the order of 20 million bits, which would result, for example, if an 8 millisecond fade occurred during a 2.5 gigabit/sec. transmission.

DETAILED DESCRIPTION OF THE DRAWING

Fig. 1 is a schematic block diagram of an optical free-space communication system using the invention;

Fig, 2 is a schematic block diagram of the components needed to perform the invention at the transmit end of the system;

Fig. 3 is a diagram illustrating the time sequencing of the incoming data stream interleaving;

Fig. 4 is a flow chart showing interleaving of 60-bit segments of successive codewords;

Fig. 5 is a diagram illustrating remapping of addresses; and

Fig. 6 is a flow chart of the process including address remapping at the transmit end.

ILLUSTRATIVE EMBODIMENT

In the exemplary embodiment described below, the principle of interleaving moderately sized burst-error correction code blocks is used, but on a macro scale much larger than conventionally applied, such that the interleaving (for the examples illustrated) spans hundreds of millions of bits in order to support recovery from burst errors on the order of tens of millions of bits. Dynamic Random Access Memory (DRAM) device technology are used by way of example, to make it feasible and economical to support the extremely large memory arrays that are required to implement such a process. The large row-column random access overhead, which is universal with DRAM technology, is substantially reduced by a virtual address remapping of physical addresses to enable operating the DRAM devices asymptotically close to the burst memory-cycle rate, which is an essential attribute when

supporting state-of-the-art high-speed optical-transmission data rates. The effect of the remapping is that overhead cycle bursts are distributed rather than occurring in clusters of consecutive memory references (which would occur if a straightforward use memory address space were applied) and allowing the high-speed memory reference rate to be maintained with minimal elasticity in the data flow.

The process draws upon prior art coding methodology, which involves first encoding the data stream into codewords or blocks of **n** bits comprising **k** payload bits and (**n-k**) error-correcting-code-bits. The process then defines the maximum number of errors that can be corrected within a codeword as **b**, taking into account that the maximum number of bits that can be corrected by any linear code is:

b = .5 *(n-k). (equation 1),

and this limit is attained for selected instances of Reed-Solomon coding.

Assume an example Reed-Solomon code of (255,223) (which means the code word is 255 *symbols* in length, of which 223 are payload symbols, 255-223 = 32 are check symbols, and the symbol is an eight-bit octet). The bound of correctable indicated by Equation 1 is achieved for this example, which indicates up to .5 * (255-223) = 16 symbols can be corrected. This means the codeword size in bits is 8*255 = 2040 for this example, and that an error burst in one codeword of up to b = 16 x 8 =128 bits could be corrected. If the objective is to mask error bursts of duration E bits, the number of codewords, M, that must be interleaved is:

M=E/b. (equation 2)

Thus, correcting an error burst of the order of 20 million bits would require interleaving

$$M = 20 \times 10^6/128 = 156{,}250 \text{ codewords.}$$

The span of the interleaving (that is, the dimension of the permutation matrix, i.e. size **S** of the buffer required and hence the duration of the latency added by this process) is:

$$\mathbf{S} = \mathbf{M^*n}. \text{ (equation 3)}$$

For the above example parameters, M is 156,250, n (expressed in bits) is 2040, such that a buffer of $M^*n = 3.1875 \times 10^8$ bits is required.

The invention is illustrated as part of an optical free-space transmission system seen in FIG. 1. The system receives at an input end a data stream payload 10. The payload may be in the form of a continuous data stream; or may comprise data bursts where the bit-length of the payload may vary from burst to burst. The burst-error correction process may be applied unconditionally and continuously to all data transmitted; or may be selectively applied when conditions warrant. *The free-space medium conditions measured by sensors 19 may include, for example, humidity, temperature, cloud coverage, crosswind, ________ and ________. Sensors 19 may be linked to computer controller 26, where instructions are contained which specify the one or more transmission medium conditions which sensors 19 will detect.* If the *free-space medium scintillation-causing* conditions are present, data payload 10 is routed through signal conditioner 11. Here, the data is encoded, interleaved and buffered in a manner to be

described. The output of signal conditioner 11 is transmitted by transmitter s12 through free-space medium 13 to a receiver 14. If the received signal has been conditioned for scintillation, it is fed to signal extractor 15 for decoding and de-interleaving before being routed for end use in video or high-speed data applications.

Referring now to Fig, 2, signal conditioner 11 comprises encoder/interleaver 20 which preferably is of the Reed-Solomon type. A data stream payload 10 of 2.5 gbit is fed to Reed-Solomon encoder/interleaver 20, which outputs a 2.86 gbit stream. Encoder/interleaver 20 encodes the payload data stream 10 into codewords, each of length **n** as seen in Fig. 3. The interleaving process is equivalent to a matrix transpose; that is, (for the set of numbers used in this instance) a matrix of 156,250 rows x 34 columns, with each matrix entry a 60-bit section. A 60-bit shift register 21 receives the encoder/interleaver 20 output. Sixty-bit sections of the codeword are chosen because 60 is an integer factor of 2040 (a useful but not essential property), and 60 bits x 156250 x 2 is close to the nominal 20 megabit burst-error length objective of 18.75 megabits. A burst error of 18.75 million bits would destroy two 60-bit sections (120 bits) in each of 156,250 interleaved codewords, but because all of the codewords have the capability of correcting 128 bits, all the data would be recovered in the example.

Input shift register 21 distributes the fragments created in encoder/interleaver 20 to a buffer store 22 comprising a bank of eight SDRAMs 22a....22h, ganged in groups of four. The SDRAMs are 16 bit X 8 megaword stores. The SDRAM devices are loaded in accordance with addresses supplied by Field Programmable Gate Array (FPGA) configured

as address generators 23, 24. READOUT from the SDRAM devices is to output shift register 25, which feeds transmitter 12 with a stream of encoded and interleaved bits.

Referring again to Fig. 3, the exemplary codeword 30 is split into a desired number of fragments, for illustration, six fragments 30a-f. The next codeword then is similarly fragmented; and the fragments are interleaved with the fragments 30a-f. The interleaving of codewords occurs over a span sufficiently large that the burst error of length **E** bits will affect at most **b** bits in any given codeword.

The encoding and interleaving processes performed in encoder/interleaver 20, the addressing functions of address generators 23, 24 the storage functions of SDRAMs 22a..h, and the operation of input and output shift registers 21,25 may be separate hardware components with functionalities coordinated by instruction code run in computer controller 26 shown in Fig. 2. If hardware is preferred, suitable commercially available components are: Vitesse Semiconductor VSC 7146 device for the shift registers 21, 25; and Lucent Technology's ORCA FPGA ORT8850 components for the address generators 23, 24. The functions of address generators 23, 24 and input shift registers 21,25, as well as encoder 26, may alternatively be provided as code instructions under the control of computer controller 26. In the experimental procedure of the example provided herein, the functionalities of components 20, 21, 23, 24, and 25 were provided by __________. The computer controller used in the example was a ______________________________. [Inventors: I'll contact you for possible advice on filling in these blanks.]

Preferably, Reed-Solomon coding is used having a Galois Field of 8-bit symbols and a (255,223) code configuration. Reed-Solomon coding is comprehensively described in the text: *Error Correcting Codes,* Perterson and Weldon, MIT Press, ______(date of publication) which is hereby incorporated by reference.

In the present example, a codeword is 255 octets (bytes) in length, of which 223 are payload, with the remaining 32 as check symbols. The code has the capability of correcting 32/2 or 16 bytes of error. This means that as few as 16 isolated errors (i.e. if each error were in a different octet) could be corrected; but that as many as 16 x 8 or 128 bit errors would be corrected in any block if the errors all occurred within 16 bytes.

Fig. 4 shows how segments of each codeword may be denoted by a 2-tuple where **n** is the codeword number and **m** is a 60-bit segment within the denoted codeword. After being labeled, the first block of 156,250 codewords are interleaved. After interleaving of this first block of 156,250 codewords, the codeword sequence is shown in Fig. 4, where the brackets clarify the writing of “column entries” for subsequent READOUT as rows. Consecutive entries from the same codeword are separated by 60x156,250=9.375 megabits. Thus, an erasure of any two of the bracketed sequences (each being 9.375 megabits) incurs no more than 120 megabits of error in any codeword.

A field measurement of free-space optical transmission over a 10 km range indicated roughly 90% of the fades were of duration less than 8 ms. A data

stream bit rate of 2.5 x 109 /sec. would yield a value of **E** = 20 x 10^6 bits lost during an 8 ms. fade. Since at most 128 bits of any codeword can be lost due to the burst error and still mask the burst, the number of codewords that must be interleaved in this example is:

E / b = 2 x 107/128 = 156250 (equation 4)

Since the codeword is 255 x 8 = 2040 bits long, the interleaving buffer size is:

(E/b)*n = 156250* 2040= 318,750,000 bits (equation 5)

A buffer store of this size may be realized by using SDRAMs of 128 or 256 megabits in size.

The WRITE process to SDRAM devices requires forming 60-bit words in 20.8 ns. (60 times the bit period of the 2.8 x 109 bit/sec. encoded data stream). In order to realize this performance with the minimum of overhead operations in SDRAM devices 22, it is desirable to use Class-2 SDRAM with a maximum clock rate of 133 MHz., or 7.5 ns. cycle time. However, this seven cycle WRITE epoch is not compatible with 20.8 ns. READOUT rate at which new 60-bit codeword sections are being generated.

To overcome this incompatibility, it has been realized that state-of -the-art SDRAM devices can READ or WRITE at the device cycle rate within a page (i.e. row). For example, for the Micron Technologies SDRAM, device no. MT48LC8M16A2, revision 11/99, p 50.) (with 16 bits x 2M x 4 banks) the page size is 512 sixteen-bit words, and the clock rate is 133 MHz. (7.5 ns.).

Therefore, when addressed in a straightforward way, SDRAM devices 22 would require 7 x 7.5 = 52.5 ns. per WRITE (because the WRITE address increment far exceeds the page size) while consecutively-addressed READ operands could asymptotically be performed at a 7.5 ns. rate, well under the 20.8 ns. rate required.

It may be seen that in the above example, the "READ" vs. the "WRITE" rates are unequal, which is a disadvantage. In accordance with another aspect of the invention, the READ vs. WRITE rates may be equalized, which allows the process to be workable in real time with a minimum number of SDRAM memory devices. This result may be achieved by remapping memory addresses in the manner next described.

The remapping strategy is illustrated in FIG. 5 memo. Essentially, the idea is to:

1. regard each page in SDRAM memory as multiple "virtual" pages, and
2. exploit the fast WRITE rate on the same (physical) page in exchange for requiring a more frequent page change during READ in the permutation operation.

Referring to FIG. 5, the general approach is to WRITE K consecutive entries into one physical page, with the result that the READ process must then change pages [P/K] times as often (where P is the page size) compared with simply READING each P-entry page of SDRAM as a single sequence of consecutive addresses.

For the numbers involved in the above example, we define each physical 512-word SDRAM page as consisting of 34 pages of 15 words each (two words are wasted). Recall that the permutation matrix is 34 x 156250 in size, and therefore 34 is selected to make indexing systematic. In this particular combination of numbers, the "WRITE" process in the interleaving operation does not have to change pages at all before a physical page is full.

During the WRITE operation, entries 1,1 1,2....1,34 are stored in physical addresses 0,15,....,495 of the first SDRAM page, but these are to treated during "READ" as addresses 0, 156250,.....,33x156250 respectively. Because the factorization of addresses maps has the row length as one factor, exactly 15 rows of 34 entries fit in one first physical page. [Inventors: does the previous sentence make technical and grammatical sense? Pls. check.]The "virtual" addresses referred to in Fig. 5 refer to the sequence in which the READOUT is performed to complete the permutation.

Because of the 7-cycle overhead when a page change does occur (at 7.5 ns/cycle) versus the 20.8 ns. system cycle rate, a first-in-first-out elastic memory of 4 entries provides a means to bridge the page change. The 52.5 ns. interruption incurred by the page change is effectively masked with a backlog of 3 entries in the elastic memory.

The flow chart of Fig. 6 describes the key process steps including a summary of the remapping of SDRAM addressing to provide a balance of READ vs. WRITE operations. [Note to ceg and inventors: we will need to

re-visit this flowchart to make sure the claims, once written, can be read on the flowchart.]

The effects of scintillation degradation in free-space optical transmission can vary as a function of many ambient conditions. For example, for a point-to-point optical range of 4.4 km. and a crosswind on the order of 10 mph, the temporal correlation of scintillation is on the order of 15 milliseconds. For a range of 1km. and 10 mph crosswind, the time scale is 7-8 milliseconds. If the crosswind is on the order of 20 mph in the range of 1km., the temporal correlation becomes about 4 milliseconds. The extent of scintillation effect also varies as a function of other atmospheric conditions including, for example, air temperature, emissions and relative humidity.

At the receiver end of the optical free-space system shown in Fig. 1, a signal generated in computer controller 26 instructs receiver 14 as to whether the incoming signal is conditioned for scintillation or not. If conditioned, receiver 14 outputs the received signal to signal extractor 15. The decoding and de-interleaving process may be performed in software in an associated processor (not shown) with code instructions keyed to the encoding, interleaving and remapping processes performed in Fig. 2 (should we provide brief further explanation?______________________. inventors, I need to talk to you for advice on how much we need to tell the skilled reader about how to write the code for the receiver end and , for that matter, the transmit end.)

Claims:

Claim 1. A process for optical free-space communications wherein the communications medium is subject to intervals of burst error due to atmospheric scintillation, said process comprising the steps of:

encoding a transmission payload data bit-stream into codewords;

fragmenting each of a selected series of said codewords into sections;

interleaving corresponding said sections of said codewords over a substantial span of said payload data-bit stream that is large compared to an anticipated burst error interval;

WRITING said interleaved sections into designated addresses of a permutation buffer comprising banks of SDRAM devices arrayed as a matrix of megaword stores with physical row-and-column addresses wherein each said row constitutes a page, each said SDRAM device having a burst memory cycle rate;

establishing "virtual" addresses by designating each physical row in SDRAM memory as multiple "virtual" pages;

mapping said virtual addresses onto said physical addresses of each said SDRAM device;

READING OUT from said banks of SDRAM devices the content of said actual addresses in a sequence determined by the re-mapped "virtual" pages, said sequence being chosen in such a way that the processing overhead associated with row-address changes is roughly equal in both said WRITE step and said READING OUT step, thereby to enable each said SDRAM device to operate asymptotically close to its burst memory cycle rate; and

transmitting into said communications medium the encoded and interleaved data-bit stream of said READING OUT step.

Claim 2. The process of claim 1, further comprising the step of decoding said encoded and interleaved data-bit stream at a remote receiver to recover said transmission payload data bit-stream.

Claim 3. The process of claim 2, wherein the step of encoding of said transmission payload data bit-stream into codewords is effected using Reed-Solomon coding.

Claim 4. The process of claim 3, comprising the further step of sensing conditions in said communications medium which cause scintillation effects; and activating said encoding step when said conditions are detected.

Claim 5. The process of claim 4, wherein the number of sections into which each said codeword is fragmented is in the range of from 2 to 6, and wherein the respective said sections of each said codeword are

interleaved with the corresponding sections of the adjoining said codeword.

Claim 6. The process of claim 5, wherein each said virtual page is substantially from ____ to ______ codewords in length.

Claim 7. The process of claim 6, wherein said WRITE step comprises writing K consecutive entries into one physical page of size P, and said READING OUT step comprises changing pages [P/K] times as often (inventors: does 'as often' mean 'more frequently'?) compared with reading each P-entry page of SDRAM as a single sequence of consecutive addresses

Claim 8. A communications process wherein the communications medium is subject to intervals of burst error, said process comprising the steps of:

encoding a transmission payload data bit-stream into codewords;

fragmenting each of a selected series of said codewords into sections;

creating a new data-bit stream by interleaving corresponding said sections of said codewords over a substantial span of said payload data-bit stream that is large compared to an anticipated burst error interval;

WRITING said interleaved sections into designated addresses of a permutation buffer comprising banks of memory devices arrayed as a

matrix of megaword stores with physical row-and-column addresses wherein each said row constitutes a page, each said SDRAM device having a burst memory cycle rate;

establishing "virtual" addresses by designating each physical row in said memory devices as multiple "virtual" pages;

mapping said virtual addresses onto said physical addresses of each said memory device;

READING OUT from said banks of said memory devices the content of said actual addresses in a sequence determined by the re-mapped "virtual" pages, said sequence being chosen in such a way that the overhead associated with row-address changes is roughly equal in both said WRITE step and said READING OUT step, thereby to enable each said memory device over time to consistently operate asymptotically close to its burst memory cycle rate; and

transmitting into said medium the encoded and interleaved data-bit stream of said READING OUT step.

Claim 9. The process of claim 8, wherein said memory devices are SDRAM buffer stores.

Claim 10. The process of claim 9, further comprising the step of decoding said encoded and interleaved data-bit stream at a remote receiver to recover said transmission payload data bit-stream.

Claim 11. The process of claim 10, wherein the step of encoding of said transmission payload data bit-stream into codewords is effected using Reed-Solomon coding.

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"H"

X-Sender: jgraves@pop-server.austin.rr.com
Date: Mon, 5 Feb 2001 23:32:59 -0600
To: rshively@lucent.com
From: Chuck Graves <jgraves@austin.rr.com>
Subject: final patent corrections

Dick Shively,

I have made all the minor corrections per your 1/17 email. However, I want to make sure I understand your email explanation for the changes , and also the implications of your replacing the text starting on p. 12 line 4 through the end of page 13.

The email states" "The example was in error...recasting the explanation specifically as a matrix transpose...further led to the realization that with the example paraameters the solution at the traansmitter end did not require a tricky addressing scheme, but at the receiver it definitely does".

I need your help specifically as follows.

1. In the replacement language p. 12-13, we say that if the matrix is written as in Fig. 5A,...then in this particular example .. it is not necessary to apply the address re-mapping (in the transmitter). That may be true for the example given, but in the general case is it not a key part of the invention that we NORMALLY WOULD PERFORM address remapping at the transmitter? If so, please explain under what circumstances. Or, do we now never perform address remapping at the transmitter; and if so , why is that?

2. In the replacement language and in new Fig. 5, we no longer use the term "virtual addresses". This being so, don't we need to eliminate the term "virtual addresses" from elsewhere in the spec as on p. 3 line 5 et seq; and also from the claims? If not, is the current text that uses the term "virtual addresses" in need of any revisions?

3. What, simply stated, is the difference between old Fig. 5 and new Fig. 5A, 5B? insofar as the processing of information?

4. In light of your replacement text in the specification what corrections should be made, or what text should be substituted, for p. 4, lines 5-15 in the Summary of the Invention? Conforming the Sumnmary to the new explanation is critically important because tthe Summary is what distinguishes the invention from the prioir art. Also, the claims need to be consistent with the Summary. Don't worry about the claims - when you're satisfied with the (revised?) Summary I will conform the claims.

I eagerly await your words of wisdom. And yes, a good time was had in Tampa.
Thanks, Dick-

Charlie G. 2/6/2001 11PM.